AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-4. (Canceled)

5. (Currently Amended) A method of producing a chip scale package, comprising:

~~providing an wafer, the wafer comprising a plurality of integrated circuit chips, each integrated circuit chip comprising~~

~~a plurality of bond pads aligned on an upper surface of the integrated circuit chip and~~

~~a plurality of conductive bumps formed on the plurality of bond pads;~~

~~dicing the wafer into a plurality of chip arrays, each array comprising two mo more integrated circuit chips;~~

mounting ~~each~~ an array of integrated circuit chips on a substrate, each integrated circuit chip comprising:

a plurality of bond pads on an upper surface of integrated circuit chip, wherein each of said bond pads is aligned in a central row, and

a plurality of conductive bumps formed on the plurality of bond pads;

such that the bumps align with corresponding solder pad openings on an upper surface of the substrate;

reflowing the integrated circuit chips of each array, thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate;

under fill encapsulating the integrated circuit chips and the substrate; and

dicing the array, joined to the substrate, into individual chip scale packages, each comprising only one integrated circuit chip.

6. (previously presented) The method according to claim 5, further comprising:

prior to mounting each array on a substrate, dipping each array in flux material, such that flux material adheres to the bumps;

wherein, when each array is mounted on a substrate, the flux material adheres the bumps to the solder pad openings.

7. (previously presented) The method according to claim 6, further comprising:

after reflowing the integrated circuit chips, cleaning the integrated circuit chips, the bumps, and the substrate to remove flux material.

8. (previously presented) The method according to claim 5, wherein:

under fill encapsulating the integrated circuit chips comprises injecting encapsulation material into a gap between the integrated circuit chips and the substrate.

9. (previously presented) The method according to claim 5, further comprising:

before dicing the array into individual chip scale packages, forming solder balls, conductively connected to the bumps, on the under surface of the substrate.

10-12 (cancelled)

13. (new). The method according to claim 5, further comprising:

prior to mounting each array on a substrate, providing a wafer comprising a plurality of integrated circuit chips; and

dicing the wafer into the array of integrated circuit chips, each array comprising two or more integrated circuit chips.

14. (new) A method of producing a chip scale package, comprising:

mounting an array of integrated circuit chips on a substrate, each integrated circuit chip comprising:

a plurality of bond pads on an upper surface of integrated circuit chip, wherein each of said bond pads is aligned in a plurality of central rows, and

a plurality of conductive bumps formed on the plurality of bond pads;

such that the bumps align with corresponding solder pad openings on an upper surface of the substrate;

reflowing the integrated circuit chips of each array, thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate;

under fill encapsulating the integrated circuit chips and the substrate; and

dicing the array, joined to the substrate, into individual chip scale packages, each comprising only one integrated circuit chip.

15. (new) The method according to claim 14, further comprising:

prior to mounting each array on a substrate, dipping each array in flux material, such that flux material adheres to the bumps;

wherein, when each array is mounted on a substrate, the flux material adheres the bumps to the solder pad openings.

16. (new) The method according to claim 15, further comprising:

after reflowing the integrated circuit chips, cleaning the integrated circuit chips, the bumps, and the substrate to remove flux material.

17. (new) The method according to claim 14, wherein:

under fill encapsulating the integrated circuit chips comprises injecting encapsulation material into a gap between the integrated circuit chips and the substrate.

18. (new) The method according to claim 14, further comprising:

before dicing the array into individual chip scale packages, forming solder balls, conductively connected to the bumps, on the under surface of the substrate.

19. (new). The method according to claim 14, further comprising:

prior to mounting each array on a substrate, providing a wafer comprising a plurality of integrated circuit chips; and

dicing the wafer into the array of integrated circuit chips, each array comprising two or more integrated circuit chips.